REMARKS

Reexamination and reconsideration are respectfully requested in view of the following remarks.

35 U.S.C. § 103

The Office Action rejects claims 1-20 under 35 U.S.C. § 103 over Yard et al. U.S. Patent 5,896,393 ("Yard") in view of Hazen U.S. Patent 5,379,413 ("Hazen").

Applicant respectfully traverses those rejections for at least the following reasons.

Claim 1

Among other things, the method of claim 1 includes erasing the entire physical array and writing first data back into the physical array after erasing the entire physical array.

The Office Action fairly admits that Yard does not disclose such features.

However, the Office Action states that Hazen discloses such features and that it would have been obvious to one of ordinary skill in the art at the time the invention as made to modify Yard to include such features, supposedly because of the laundry-list of reasons listed in the Office Action at page 4, lines 6-16.

Applicant respectfully traverses the proposed combination of Yard and Hazen as lacking any suggestion or motivation in the prior art, and further traverse any proposed modification of Yard that would erase the entire physical array as being contrary to the fundamental principles of Yard.

At the outset, M.P.E.P. § 2142 states that "there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." Similarly, M.P.E.P. § 2143.01 provides that:

> "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is

> some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art."

Here, the Office Action has not cited anything in the prior art in support of the supposed motivation to modify Yard that is set forth at page 4, lines 6-16, nor did the Examiner submit an affidavit as required by 37 CFR 1.104(d)(2) if this proposed motivation were based on facts within his personal knowledge (see MPEP § 2144.03). Applicant requests such an affidavit if this rejection continues to be maintained based a motivation for combination not explicitly suggested in the prior art.

Additionally, M.P.E.P. § 2143.01 provides that:

> "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious."

Here, Applicant respectfully traverses any proposed modification of Yard that would erase the entire physical array, as such a modification would be clearly contrary to the fundamental principles of Yard.

Yard teaches that the physical memory array 12 is to be assigned into two logical portions: a "storage array" and an "update array" (Yard at col. 4, lines 36-40 and FIGs. 12-14). During an update procedure of Yard's invention, the active (undeleted) data files are copied to the update array portion of the physical array, and then the sectors comprising the storage array portion of the physical array are erased (Yard at col. 5, lines 7-13 and FIG. 8). That is, Yard requires that a portion of the physical memory array 12 (the "update array" portion) always be maintained to store data. Therefore, it would destroy the fundamental principles of Yard's invention to somehow modify Yard's method to erase the entire physical array – including the "update array" sectors.

Accordingly, Applicant respectfully traverse any such proposed modification of Yard.

Furthermore, Applicant respectfully submits that any proper modification of Yard based on the cited teaching of Hazen would not produce the method of claim 1. Hazen states that:

> "**Because these source terminals are all connected to one another by metallic busing in the array**, the entire array must be erased at once."

Hazen at col. 1, lines 39-41 (emphasis added).

That is, as indicated by Applicant in the Response to the previous Office Action filed on 20 December 2004:

> "Hazen when referring to erasing an entire array is thus referring to all the memory cells connected to a common source line (e.g., to one sector of a multi-sector Flash memory)."

In that regard, Applicant notes that the Examiner has misunderstood what Applicant meant by the above parenthetical statement. Contrary to the statement in the Office Action at page 11, lines 4-7, Applicant did **NOT** "admit" that "Hazen teaches a multi-sector flash memory," as indeed that is not what Hazen discusses. Instead, what Applicant was trying to say was that the principle which Hazen discusses in the cited text would only apply to one sector of a multi-sector Flash memory array, such as that disclosed and discussed by Yard, because Hazen's underlying predicate ("**these source terminals are all connected to one another by metallic busing**") only applies to one sector in a multi-sector Flash memory array.

More specifically, if one attempted to somehow combine Hazen's "teaching" regarding a flash array lacking separate sectors, to Yard's multi-sector array, one would only come to the conclusion that an entire **sector** of Yard's device "must be erased at once" "because **these** source terminals are all connected to one another by metallic busing in the array." There would be nothing in Hazen's statement that would suggest that Yard's entire array "must be erased at once" (or even should be erased at once), especially considering that Yard very specifically teaches that individual sectors are erased separately.

Therefore, Applicant respectfully submits that any proper modification of Yard based on the cited teaching of Hazen would not produce the method of claim 1.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 1 is patentable over the prior art.

Claims 2-11

Claims 2-11 depend from claim 1 and are deemed patentable over the prior art for at least the reasons set forth above with respect to claim 1, and for the following additional reasons.

Claim 2

Among other things, in the method of claim 2 the temporary storage is external to the semiconductor memory.

Applicant respectfully submits that no such feature is disclosed or suggested by any combination of the cited art.

The Office Action states at page 5, lines 1-4, that Yard discloses such a feature. However, the Office Action fails to provide any support or citation for its statement that "the temporary storage is external to the semiconductor memory."

Applicant respectfully submits that Yard very clearly teaches that the "temporary storage" is the update array which is internal (and indeed, integral) to the semiconductor memory, and not external thereto (see e.g., Yard at col. 4, lines 36-40 and FIGs. 12-14).

Therefore, Applicant respectfully submits that the cited prior art, alone or in combination, does not disclose or suggest a method where the temporary storage is external to the semiconductor memory.

Accordingly, for at least this additional reason, Applicant respectfully submits that claim 2 is patentable over the prior art.

Claim 3

Among other things, the method of claim 3 comprises simultaneously erasing all memory cells in the physical array.

As explained above with respect to claim 1, the fundamental principle of Yard involves copying data from a first portion of the physical array to a second portion of the physical array before erasing the first portion of the physical array, so that the data may be saved. If one were to somehow try to modify Yard to simultaneously erase all memory cells in the physical array, this fundamental principle would clearly be destroyed. Therefore, any such proposed modification of Yard would be improper under M.P.E.P. § 2143.01.

Accordingly, for at least this additional reason, Applicant respectfully submits that claim 3 is patentable over the prior art.

Claim 4

Among other things, the method of claim 4 comprises erasing all of the sectors in the physical array.

As explained above with respect to claim 1, the fundamental principle of Yard involves copying data from a first portion of the physical array to a second portion of the physical array before erasing the first portion of the physical array, so that the data may be saved. If one were to somehow try to modify Yard to erase all of the sectors in the physical array, this fundamental principle would clearly be destroyed. Therefore, any such proposed modification of Yard would be improper under M.P.E.P. § 2143.01.

Accordingly, for at least this additional reason, Applicant respectfully submits that claim 4 is patentable over the prior art.

Claim 6

In the method of claim 6, data from different data blocks is written back into the physical array at consecutive addresses in the physical array without regard to boundaries between sectors.

Applicant respectfully submits that no such feature is disclosed or suggested by any combination of the cited art.

The Office Action states at page 5, lines 1-4, that Yard discloses such a feature at col. 5, lines 15-17.

Applicant respectfully disagrees.

The cited text of Yard at col. 5, lines 15-17 discloses that when the storage array portion of the physical memory array 12 is reassigned, it will begin at the first array location of the first active file. The text does not state anything about writing different data blocks back into the physical array at consecutive addresses in the physical array without regard to boundaries between sectors. Indeed, Yard does not technically write any data "back" into the physical array, but to the extent that Yard copies data to new locations in the physical array, that data is not even written into the storage array portion, but instead is copied into the update array portion. And Yard teaches that the update array portion **is** governed by sector boundaries (see, e.g., col. 5, lines 17-19; col. 7, lines 33-40, 49-51; and FIGs. 12-14).

Accordingly, for at least this additional reason, Applicant respectfully submits that claim 6 is patentable over the prior art.

Claim 12

Among other things, the system of claim 12 includes: (1) a first memory; (2) a storage device; and (3) a processor executing a file management procedure that reads data blocks from an array in the first memory and stores them in the storage device.

Applicant respectfully submits that no system having this combination of features is disclosed or suggested by any combination of the cited art.

At the outset, the Office Action states that FIG. 1 of Yard supposedly shows the recited storage device, but the Office Action does not point to any element that allegedly corresponds to this storage device.

Applicant respectfully submits that Yard does not disclose the recited storage device in FIG. 1 or elsewhere. The recited storage device stores data blocks read from an array in the first memory during a file management procedure. Yard does not disclose that any data blocks read from its memory array are stored in a separate storage device during a file management procedure. In particular, contrary to the Office Action, Yard does not disclose such a storage device at col. 5, lines 7-10.

Instead, Yard very clearly teaches that teaches that it stores the data blocks in the update array portion which is internal (and indeed, integral) to the memory array 12, and not in any separate storage device of a computer system (see e.g., Yard at col. 4, lines 36-40 and FIGs. 12-14). So, Applicant respectfully submits that the cited prior art, alone or in combination, does not disclose or suggest the system of claim 12 including; (1) a first memory; (2) a storage device; and (3) a processor executing a file management procedure that reads data blocks from an array in the first memory and stores them in the storage device.

Therefore, the cited prior art cannot produce the system of claim 12.

Also among other things, the system of claim 12 includes a processor that executes a file management procedure that: (i) reads data blocks from an array in the first memory and stores them in the storage device; (ii) erases the array in its entirety; and (iii) writes the data from the storage device back into the first memory.

The Office Action fairly admits that Yard does not disclose erasing the array in its entirety; and writing the data from the storage device back into the first memory.

However, the Office Action states that Hazen discloses such a feature and that it would have been obvious to one of ordinary skill in the art at the time the invention as made to modify Yard to include such features, supposedly because of the laundry-list of reasons listed in the Office Action at page 8, lines 11-21.

As explained above with respect to claim 1, Applicant respectfully traverses the proposed combination of Yard and Hazen as lacking any suggestion or motivation in the prior art, and further traverse any proposed modification of Yard that would erase the entire array as being contrary to the fundamental principles of Yard. As also explained above with respect to claim 1, Applicant also respectfully submits that any proper modification of Yard based on the cited teaching of Hazen would not produce the system of claim 12 including a procedure executing the recited file management procedure.

Accordingly, for at least these reasons, Applicant respectfully submits that the system of claim 12 is patentable over the prior art.

Claims 13-20

Claims 13-20 depend from claim 12 and are deemed patentable over the prior art for at least the reasons set forth above with respect to claim 12, and for the following additional reasons.

Claim 17

Among other things, the system of claim 17 includes a processor that executes a file management procedure that simultaneously erases all memory cells in an array of a first memory.

As explained above with respect to claim 1, the fundamental principle of Yard involves copying data from a first portion of the array to a second portion of the array before erasing the first portion of the array, so that the data may be saved. If one were to somehow try to modify Yard to simultaneously erase all memory cells in the array, this fundamental principle would clearly be destroyed. Therefore, any such proposed modification of Yard would be improper under M.P.E.P. § 2143.01.

Accordingly, for at least this additional reason, Applicant respectfully submits that claim 17 is patentable over the prior art.

Claim 18

Among other things, the system of claim 18 includes a processor that executes a file management procedure that erases all of the sectors in the array of a first memory.

As explained above with respect to claim 1, the fundamental principle of Yard involves copying data from a first portion of the array to a second portion of the array before erasing the first portion of the array, so that the data may be saved. If one were to somehow try to modify Yard to erase all of the sectors in the array, this fundamental principle would clearly be destroyed. Therefore, any such proposed modification of Yard would be improper under M.P.E.P. § 2143.01.

Accordingly, for at least this additional reason, Applicant respectfully submits that claim 18 is patentable over the prior art.

Claim 20

Among other things, the system of claim 20 includes a processor that executes a file management procedure that writes data back into the array at consecutive addresses in the array without regard to boundaries between sectors.

Applicant respectfully submits that no such feature is disclosed or suggested by any combination of the cited art.

The Office Action states at page 10, lines 6-8, that Yard discloses such a feature at col. 7, lines 46-51.

Applicant respectfully disagrees. The cited text does not state anything about writing data from different data blocks into the array at consecutive addresses in the array without regard to boundaries between sectors. Indeed, the cited text teaches that data is written into the array **with** regard to sector boundaries – the write address register 34 is set "to the first addressable location of the sector to which end-array 26 is pointing" (emphasis added). See also, e.g., Yard at col. 5, lines 17-19; col. 7, lines 33-40; and FIGs. 12-14.

Accordingly, for at least this additional reason, Applicant respectfully submits that claim 20 is patentable over the prior art.

CONCLUSION

In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 1-20, and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283-0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No.

50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

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